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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application for inventor(s):

MASAYUKI ISHIKAWA, HIDEAKI KOHZU and YUKIO NAITO

For: PIEZOELECTRIC OSCILLATOR

Also enclosed are:

- 7 sheets of drawings
- Certified copy of Japanese Patent Application No. 11-289298 of October 12, 1999 on which Convention priority is claimed (to follow)
- Declaration and Power of Attorney
- Verified Statement Claiming Small Entity Status
- Information Disclosure Statement by Applicant
- Preliminary Amendment
- An assignment of the invention to TOYO COMMUNICATION EQUIPMENT CO., LTD.

CALCULATION OF FEES								
ITEM		TOTAL NO. OF CLAIMS		NO. OF CLAIMS OVER BASE	LG/SM \$ ENTITY FEE		\$ AMOUNT	\$ FEE
A	TOTAL CLAIMS FEE	6	-20	0	LG=\$18 SM=\$9	\$18	\$ 0	
B	INDEPENDENT CLAIMS FEE*	5	-3	2	LG=\$80 SM=\$40	\$80	\$ 160	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)							\$ 160
D	MULTIPLE-DEPENDENT CLAIMS FEE							LARGE ENTITY FEE = \$270 SMALL ENTITY FEE = \$137
E	BASIC FEE							LARGE ENTITY FEE = \$710 SMALL ENTITY FEE = \$355
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)							\$ 870
G	ASSIGNMENT RECORDING FEE							\$ 40
	*LIST INDEPENDENT CLAIMS 1							

- The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 11-1445. A duplicate copy of this sheet is enclosed.
- A check in the amount of \$ 870 to cover the filing fee is enclosed.
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Inventor(s): MASAYUKI ISHIKAWA, HIDEAKI KOHZU and YUKIO NAITO

For: PIEZOELECTRIC OSCILLATOR

## PIEZOELECTRIC OSCILLATOR

## BACKGROUND OF THE INVENTION

## Field of the Invention

5       The present invention relates to a piezoelectric oscillator and, more particularly, to a piezoelectric oscillator that uses a MOS capacitance element.

## Description of the Related Art

10      Various forms of circuits have hitherto been proposed and put to practical use as an oscillator that uses a piezoelectric resonator that is represented by a crystal resonator. They are being used in a wide variety of electronic appliances, for example, as signal sources of portable  
15      telephones, computers, etc.

On the other hand, in each of such oscillators, for achieving various objects that include making adjustments of the frequency at the time of the manufacture, realizing the channel-frequency-adjusting function or AFC (automatic  
20      frequency control) function, etc. and that further include making compensations for the frequency in connection with the temperatures, conforming the oscillator to a large number of channel frequencies, etc., it is indispensable to use a variable-capacitance element.

25      As a circuit that can realize such objects, there is generally used a circuit that is illustrated in, for example,  
Fig. 6.

The oscillation circuit illustrated in the figure is an ordinary circuit of the crystal oscillator using an inverter amplifier. In this oscillation circuit, between an input and an output of an inverter amplifier 101 there is inserted a parallel circuit comprised of a crystal resonator 102 and a feedback resistor R1. Also, between the input and the output thereof and the ground there are inserted a capacitor C1 and a capacitor C2, respectively. Simultaneously, to either one of the capacitor C1 and the capacitor C2 (in this example to the capacitor C1) there is connected a variable-capacitance diode D1 serving as a variable-capacitance element. And, a cathode of the variable-capacitance diode D1 and a control terminal Vcont are connected to each other via a resistor R2 for preventing the flow of direct currents.

Because the operation of this oscillation circuit is well known, it is thought unnecessary to newly give an explanation of it. Briefly explaining, however, in this oscillation circuit, according to a direct current voltage that is applied to the control terminal Vcont, the capacitance value of the variable-capacitance diode D1 varies. For this reason, by controlling this control voltage, it is possible to perform various kinds of adjustments of the frequency, for example, AFC and so forth as mentioned above.

On the other hand, in view of the recent demands for miniaturization, and reduction in the power consumption, of various kinds of electronic appliances, there has been also a demand for conversion of the above-described oscillator to

an IC version.

However, in a case where converting the oscillation circuit including the variable-capacitance diode D1, such as that illustrated in Fig. 6, to an IC version, this diode cannot  
5 but be formed using a process step different from that for forming other semiconductor circuits. Therefore, this diode has been an obstacle to cheaply converting the oscillation circuit to an IC version.

Namely, the variable-capacitance diode D1 which is a  
10 bipolar type of semiconductor must be formed using a process step separate from that for forming the inverter amplifier 101 which is generally a C-MOS type of semiconductor. Therefore, the process for such formations is not only complex but the IC product was high in cost.

15 On the other hand, as a variable-capacitance element suited to conversion to IC version, there is known a MOS type variable-capacitance element, the utilization of that has been in expectation.

As a crystal oscillator using such a MOS type  
20 variable-capacitance element, there is the one that is disclosed, for example, in Japanese Patent Application Laid-Open No. 10-13155 entitled "Crystal Resonator with Frequency-Adjusting Function".

This crystal oscillator is constructed as follows. As  
25 illustrated in Fig. 7, between an input terminal and an output terminal of an inverter amplifier 101 there is inserted a parallel circuit comprised of a crystal resonator 102 and a feedback

resistor R1. A MOS type variable-capacitance element 103 is connected to the input terminal of the inverter amplifier. And, simultaneously, an electric-charge injection terminal TI of the MOS type variable-capacitance element 103 and a control terminal Vcont are connected to each other.

As the MOS type variable-capacitance element 103, although it is only a mere one example, there is known the one illustrated in Fig. 8. Namely, in this element 103, a positive or negative voltage is applied to the control terminal Vcont by using the N type substrate as a basis to thereby cause the flow of a tunnel current through the interior of  $\text{SiO}_2$  to thereby cause electrons to inject into or come out of a floating electrode 104.

Namely, for example, in a case where having applied a positive voltage to the control terminal Vcont, electrons flow out of the floating electrode 104. Therefore, the thickness of a depletion layer 105 situated near the floating electrode 104 becomes narrow, with the result that with a decrease in that thickness the depletion layer capacitance increases.

Also, in a case where having applied a negative voltage to the control terminal Vcont, the operation reverse to that mentioned above occurs. So, an explanation thereof is omitted.

However, as will be explained below, fundamentally, the MOS type variable-capacitance element can have its capacitance value varied over a wide range only with use of a positive power supply or negative power supply. For this reason, there was the drawback that almost no change in the capacitance value occurred when merely using only either a positive, or a negative,

single-polarity power supply alone.

This will hereafter be explained in a little more detail.

Fig. 9 is a graph illustrating an example of the relationship between an inter-electrode voltage and a 5 capacitance value of the MOS type variable-capacitance element.

As clear from this figure, in this example, when the terminal-to-terminal voltage varies within a range of from -1.5V to +0.5V including therein 0V therebetween, the capacitance value changes over a range covering approximately 80pF.

10 However, on the other hand, in the crystal oscillator, whereas the range within that the frequency is variable need generally be wide, it is more preferable that the capacitance value be gently varied with respect to the change in the control voltage than that sharply in order to perform high-precision 15 frequency control. For this reason, there has been a demand for a variable-capacitance element whose capacitance value varies over a wide range of control voltage.

Accordingly, in the case of the crystal oscillator such as that illustrated in Fig. 7, in order to obtain a wide range 20 of variable capacitance with use of the MOS type variable-capacitance element 103, it is necessary to use control voltage sources for applying both positive and negative voltages to the control terminal V<sub>cont</sub>. Therefore, there was the problem that the construction of the system making control of the 25 frequency became complex.

## SUMMARY OF THE INVENTION

The present invention has been made in order to solve the above-described problems and has an object to provide a small-sized piezoelectric oscillator which, while using a MOS 5 capacitance element suited to conversion to an IC version, enables obtaining a wide range of changes in the variable capacitance even with use of either a positive, or a negative, single-polarity power supply, and which facilitates the frequency control.

10 To attain the above object, according to the first aspect of the invention, there is provided a piezoelectric oscillator wherein, in an oscillator including a piezoelectric resonator, an amplifier, and a variable-capacitance element, the variable-capacitance element is a MOS type capacitance element, 15 one terminal of that is applied with an alternating current voltage, whose intermediate voltage is a V-volt voltage, and the other terminal of that is applied with a control voltage falling within a range whose intermediate value is the V-volt voltage.

20 According to the second aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal of an inverter amplifier; and divisional capacitors C1 and C2 25 are connected between respective ends of the piezoelectric resonator and the ground, by inserting a MOS type capacitance element in series with the piezoelectric resonator, one end

of the MOS type capacitance element is applied with a bias voltage which is the V-volt voltage at an output end or input end of the inverter amplifier and the other end thereof has supplied thereto a control voltage that varies within a range whose  
5 intermediate value is the V-volt voltage.

According to the third aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal  
10 of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric resonator and the ground, two MOS capacitance elements are inserted respectively on both sides of the piezoelectric resonator; one end of each of the MOS capacitance elements is  
15 applied with an alternating current voltage, whose intermediate voltage is a V-volt voltage; and the other end thereof is applied with a control voltage that varies within a range whose intermediate value is the V-volt voltage.

According to the fourth aspect of the invention, there  
20 is provided a piezoelectric oscillator wherein, in an inverter oscillator in which a piezoelectric element is connected to an input or output end of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric element and the ground, a MOS capacitance element is inserted between the piezoelectric resonator and  
25 an input end of the inverter amplifier or between the piezoelectric resonator and an output end of the inverter

amplifier; a control voltage  $V_{cont}$  is applied to the terminal  
on a connection-to-piezoelectric resonator side of the MOS  
capacitance element; and, when it is assumed that  $V$  represents  
the voltage that is a direct current bias voltage at the input  
5 end or output end of the inverter amplifier and that is applied  
to one end of the MOS capacitance element, it is arranged that  
said voltage becomes an intermediate voltage of the control  
voltage  $V_{cont}$ .

According to the fifth aspect of the invention, there  
10 is provided a piezoelectric oscillator wherein, in an inverter  
oscillator in which a piezoelectric element is connected to  
an input or output end of an inverter amplifier; and divisional  
capacitors  $C_1$  and  $C_2$  are connected between respective ends of  
the piezoelectric element and the ground, a MOS capacitance  
15 element is inserted between the piezoelectric resonator and  
an input end of the inverter amplifier or between the  
piezoelectric resonator and an output end of the inverter  
amplifier and a control voltage  $V_{cont}$  is applied to the terminal  
on the connection-to-piezoelectric resonator side of the MOS  
20 capacitance element; a direct current circuit of a resistor  
and a capacitor is inserted and connected between the terminal  
on the inverter-amplifier side of the MOS capacitance element  
and the input or output terminal of the inverter amplifier;  
and further a direct current bias voltage is applied to the  
25 terminal on the inverter-amplifier side of the MOS capacitance  
element.

According to the sixth aspect of the invention, there

is provided a piezoelectric oscillator according to the fifth aspect of the invention, wherein the amplitude level of an alternating current supplied to the MOS capacitance element is adjusted according to the value of the resistance of the  
5 direct current circuit; and when it is assumed that V represents the direct current bias voltage supplied to the terminal on the inverter-amplifier side of the MOS capacitance element, it is arranged that the direct current bias voltage V becomes an intermediate voltage of the control voltage V<sub>cont</sub>.

10

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating an embodiment of a crystal oscillator according to the present invention;

15 Figs. 2(a) and 2(b) illustrate a method of controlling the sensitivity to variable capacitance of the crystal oscillator according to the present invention, Fig. 2(a) being for illustrating a case where no control is made of the sensitivity to variable capacitance and Fig. 2(b) being for illustrating a case where control is made of the variable  
20 capacitance sensitivity;

Figs. 3(a) and 3(b) are circuit diagrams illustrating other embodiments of the crystal oscillator according to the present invention, Fig. 3(a) being a circuit diagram illustrating one of said other embodiments of the crystal oscillator according to the present invention and Fig. 3(b) being a circuit diagram illustrating the other of said other embodiments of the crystal oscillator according to the present

invention;

Fig. 4 is a circuit diagram illustrating still another embodiment of the crystal oscillator according to the present invention;

5 Figs. 5(a) and 5(b) are circuit diagrams illustrating further embodiments of the crystal oscillator according to the present invention;

Fig. 6 is a circuit diagram illustrating a conventional crystal oscillator;

10 Fig. 7 is a circuit diagram illustrating a conventional crystal oscillator using a MOS type variable-capacitance element;

Fig. 8 is a view of a sectional structure of the MOS type variable-capacitance element; and

15 Fig. 9 illustrates the relationship between a terminal-to-terminal voltage and a capacitance value of the MOS type variable-capacitance element.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 The present invention will hereafter be explained in detail on the basis of the illustrated embodiments thereof.

Fig. 1 is a circuit diagram illustrating an embodiment of a voltage-controlled crystal oscillator according to the invention.

25 The crystal oscillator illustrated in Fig. 1 has the following construction. Between input and output terminals of an inverter amplifier 1, whose power source voltage is Vcc,

there are respectively inserted in parallel a feedback resistor R1 and a series circuit consisting of a crystal resonator 2 and a resistor R2. And, between the input terminal of the inverter amplifier 1 and the ground there is inserted a capacitor 5 C1 while, on the other hand, between one end of the crystal resonator 2 and the ground there is inserted a capacitor C2. Further, between the other end of the crystal resonator 2 and the ground there is grounded via a capacitor C3 a MOS type variable-capacitance element 3 while, on the other hand, a point 10 of connection between the MOS type variable-capacitance element 3 and the capacitor C3 is connected to a control terminal Vcont via a resistor R3.

Next, the operation of the crystal oscillator having the above-described construction will be explained.

15 It is to be noted that since the operation of the inverter oscillation circuit is well known, an explanation thereof is omitted.

As apparent from the above-described explanation as well, the crystal oscillator illustrated in Fig. 1 is constructed 20 in such a form wherein one terminal of the MOS variable-capacitance element 3 is connected to the input terminal of the inverter amplifier 1. Therefore, as a result of this, to the other end of the MOS variable-capacitance element 3 there is applied a voltage whose level is  $V_{CC}/2$  that represents 25 the threshold level voltage  $V_{REF}$  of the inverter amplifier 1.

And, in a case where having supplied a direct current control voltage, whose level is from 0V to  $V_{CC}$ , to the control

terminal V<sub>cont</sub>, the terminal-to-terminal voltage of the MOS variable-capacitance element 3 varies within a range of from -V<sub>CC</sub>/2 to V<sub>CC</sub>/2 with the potential at a point of connection between the control terminal V<sub>cont</sub> and the input terminal of 5 the inverter amplifier 1 operating as a basis. Therefore, resultantly, both a positive and a negative voltage are applied to the MOS variable-capacitance element 3 as was previously explained using Fig. 9, with the result that the capacitance value thereof varies over a wide range.

10       Namely, for example, in a case where the inverter amplifier 1 operates with a power supply voltage V<sub>CC</sub>=5V, the one terminal of the MOS variable-capacitance element 3 is applied with the threshold voltage V<sub>ref</sub> of the inverter amplifier 1, whose level is V<sub>ref</sub>=2.5V. Further, at this time, when a control voltage 15 (V<sub>cont</sub>) falling within a range of from 0V to 5V is supplied to the control terminal V<sub>cont</sub> as a positive voltage, the terminal voltage V<sub>cont</sub> - V<sub>ref</sub> of the MOS variable-capacitance element 3 is controlled within a range of from -2.5V to +2.5V. Therefore, it is possible to control the value of the capacitance over 20 a wide range without using a minus power supply as in the conventional example.

The oscillation circuit according to the invention has the effects that will be explained below in addition to the above-described function and effect.

25       Namely, in the above-described construction, the MOS variable-capacitance element 3 is inserted into within a loop of oscillation. Therefore, to the terminal on the inverter

amplifier 1 side of it, there is applied an alternating current voltage, operating as an oscillation signal, the intermediate voltage of that is the threshold voltage  $V_{ref}$  whose level is  $V_{ref}=2.5V$ .

5 And, there is the phenomenon that the amplitude level of the alternating current voltage affects the sensitivity to variable capacitance of the MOS variable-capacitance element 3. By positively utilizing this property, it is possible to suppress the sensitivity to variable capacitance of the MOS  
10 variable-capacitance element 3 to an arbitrary value.

That will hereafter be explained in detail.

Here, for better understanding of the matter, it is assumed that the relationship between the terminal-to-terminal voltage and the capacitance value of the MOS variable-capacitance element be set such that, as illustrated in Figs. 2(a) and 2(b),  
15 the capacitance value varies in response to a control-voltage range of from -0.5V to +0.5V with the intra-terminal voltage of 0V as the center.

In Fig. 2(a), the solid line A illustrates the relationship  
20 between the intra-terminal voltage and the value of the intra-terminal capacitance that holds true when a direct current voltage  $V_{ref} = 2.5V$ , equal in level to the threshold voltage, is applied to one terminal of the MOS variable-capacitance element and a positive-polarity direct current control voltage  
25 about 2.5V as the center is applied to the other terminal of it. As seen, in a non-saturation region, in which the capacitance value linearly greatly varies, there is obtained

a high sensitivity to variable capacitance of  $80\text{pF/V}$  or so.

Regarding such MOS variable-capacitance element, under the assumption that the voltage  $V_{ref}$  applied thereto be a bias voltage of  $2.5\text{V}$  applied to the input terminal of the inverter amplifier 1, let's consider a case where that voltage  $V_{ref}$  is an oscillation alternating current voltage, which varies about the center voltage of  $2.5\text{V}$ , and which is fed back to the input end of the inverter amplifier 1.

First, assuming that such oscillation alternating current voltage be an alternating current voltage  $B$  whose amplitude level is much lower than the amplitude width of the voltage in the non-saturation region ( $F$ ) as illustrated in Fig. 2(a), the terminal-to-terminal capacitance value varies with a change of the half cycles on the plus side and on the minus side of the alternating current voltage  $B$ . However, resultantly, the terminal-to-terminal capacitance value becomes approximately an average value of the thus-varied values.

When in this state the control voltage  $V_{cont}$  decreases for example beyond a dotted line (a) in the figure, the half cycles on the minus side of the alternating current voltage  $B$  reach the saturation region ( $f$ ). Thereby, the amount of change in the capacitance decreases correspondingly to the half cycles on the minus side. And, the amount of change in the capacitance due to a change in voltage of the half cycles on the plus side becomes predominant. As a result of this, the intra-terminal sensitivity to capacitance value becomes low at the position where the alternating current voltage  $B$  reaches the saturation

region as indicated in a dotted line A'. As a result of this, the range of the control voltage  $V_{cont}$ , which is followed by a change in the capacitance, becomes enlarged.

On the other hand, when the amplitude level in the  
5 oscillation alternating current voltage is set to be an  
alternating current voltage C approximately equal to the width  
of the non-saturation voltage region as illustrated in Fig.  
2(b), merely slightly decreasing the terminal-to-terminal  
voltage for example is followed by the arrival of the half cycles  
10 on the minus side of the alternating current voltage C at the  
saturation region. Therefore, the amount of change in  
capacitance that corresponds to the half cycles on the minus  
side in the region of the terminal-to-terminal voltage whose  
level is lower than that of such slightly decreased  
15 terminal-to-terminal voltage becomes small. Conversely, when  
making the level of the voltage  $V_{cont}$  higher than 0V, the MOS  
type variable-capacitance element operates also similarly.  
Therefore, the capacitance sensitivity to  
terminal-to-terminal's voltage becomes wide in range as  
20 indicated in dotted line C', namely widely varies with respect  
to the terminal-to-terminal voltage. Resultantly, it is  
possible to make the variable-capacitance sensitivity to  
40pF/V.

Incidentally, in the foregoing explanation, the  
25 explanation has been made on the premise that the alternating  
current voltage C has an amplitude level substantially equal  
to the width of the voltage in the non-saturation region (F).

However, if such alternating current voltage C has an amplitude level that with respect to the non-saturation region is approximately 50% or more of the voltage level corresponding thereto, it is possible to obtain a sufficient practical  
5 variable-capacitance sensitivity.

Also, the control of the amplitude level of the alternating current voltage can be easily realized by adjusting the resistance value of, for example, the resistor R2.

Figs. 3(a) and 3(b) are circuit diagrams illustrating  
10 other embodiments of the crystal oscillator according to the present invention.

The point at which the crystal oscillator illustrated in each of Figs. 3(a) and 3(b) differs from that illustrated in Fig. 1 is that the MOS type variable-capacitance element  
15 3 is inserted into between the crystal resonator 2 and the capacitor C1 or between the crystal resonator 2 and the capacitor C2. The circuit of Fig. 3(a) is constructed in such a form wherein one terminal of the MOS type variable-capacitance element is connected to the output of the inverter amplifier 1 while the  
20 circuit of Fig. 3(b) is constructed in such a form wherein one terminal of the MOS type variable-capacitance element is connected to the input of the inverter amplifier and the other terminal thereof is connected to the control terminal Vcont via a resistor R3.

Further, if as illustrated in Fig. 3(a) a fixed resistor  
25 or variable resistor Rc is inserted into between the point E in the circuit and the ground whereby the value of this resistor

Rc is made arbitrarily settable, the voltage at the point E becomes controllable. As a result of this, the terminal-to-terminal's voltage of the MOS type variable-capacitance element is controlled, which enables  
5 adjusting the frequency of the oscillation circuit.

Fig. 4 is a circuit diagram illustrating still another embodiment of the crystal oscillator according to the present invention.

The respect in which the crystal oscillator illustrated  
10 in Fig. 4 differs from that illustrated in Fig. 3 is that the MOS type variable-capacitance element 4 is inserted into between the crystal resonator 2 and the capacitor C1 and the MOS type variable-capacitance element 5 is inserted into between the crystal resonator 2 and the capacitor C2. It is thereby arranged  
15 that either one of such MOS type variable-capacitance elements has its one terminal connected to either one of the input and output terminals of the inverter amplifier 1 and has its other terminal connected to the control terminal Vcont via a resistor R3 or R4.

20 And it is clear that with such construction a wider range of variable capacitance values is obtained. So, newly giving an explanation of that is omitted.

Figs. 5(a) and 5(b) are circuit diagrams illustrating further embodiments of the crystal oscillator according to the  
25 present invention.

The respect in that the crystal oscillator illustrated in each of these figures is characterized is that the amplitude

level of an alternating current voltage and a direct current bias voltage, which is a reference voltage, supplied to the MOS type variable-capacitance element 3, are made respectively separately adjustable.

5           Namely, the crystal oscillator is constructed as follows.

As illustrated in each of those figures, the MOS type variable-capacitance element 3 is inserted between the crystal resonator 2 and the capacitor C1 or between the crystal resonator 2 and the capacitor C2. A central point of connection between  
10 the crystal resonator 2 and the MOS type variable-capacitance element 3 is connected to the control terminal Vcont via a resistor R3. Further, the other terminal of the MOS type variable-capacitance element 3 is connected to a central point of connection in a series circuit of a resistor R5 and a resistor  
15 R6, which is connected between a power supply Vcc and the ground.

On the other hand, said other terminal of the MOS type variable-capacitance element 3, as illustrated in (a) of the figures, is connected to an output side of the inverter amplifier 1 and, as illustrated in (b) of the figures, is connected to  
20 an input side of the inverter amplifier 1, via a series circuit of a resistor R2 and a capacitor C4.

And, by constructing the circuit like that, initially, according to the relational expression of  $V_{ref} (DC) = R6 \times V_{cc} / (R5 + R6)$ , setting is performed of the reference voltage value  
25 Vref for the direct current bias voltage applied to the MOS type variable-capacitance element 3 to thereby adjust the reference capacitance value of this element 3. Thereafter,

according to the relational expression of  $V_{ref} (AC) = R5 \times R6 \times V_0 / (R5 + R6) \times (R2 + R5 \times R6 / (R5 + R6))$ , adjustment is performed of only the resistance value alone of the resistor R2. Setting is thereby performed of the amplitude of the alternating current  
5 voltage supplied to the MOS type variable-capacitance element  
3. If thereby adjusting the sensitivity to capacitance of the MOS type variable-capacitance element 3, this adjusting of the sensitivity to capacitance has no effect upon the set value  
of the reference capacitance. Resultantly, the process of  
10 adjusting the crystal oscillator is simplified.

It is to be noted that the  $V_0$  represents the amplitude level of the alternating current component of the input/output voltage of the inverter amplifier 1.

In the foregoing description, the present invention has  
15 been explained using the construction of applying the threshold voltage of the inverter amplifier 1 to one terminal of the MOS type variable-capacitance element 3. However, the invention is not limited to such construction. But the invention may have a construction wherein a fixed voltage is applied to the one  
20 terminal of the MOS type variable-capacitance element 3 with use of an external voltage or using a voltage that is produced using another voltage generation circuit, etc.

Further, although in the foregoing description the present invention has been explained taking up the oscillator using  
25 a crystal resonator as an example, the invention is not limited to such oscillator. But it is apparent that the invention may be applied to another oscillator that uses a piezoelectric

resonator other than the crystal resonator.

As has been explained above, the piezoelectric oscillator according to the present invention is constructed as described above. It therefore advantageously becomes possible to control  
5 the oscillation frequency widely and highly precisely without necessitating a complex-systematic construction for controlling the frequency.

What is claimed is:

1. A piezoelectric oscillator, wherein, in an oscillator including a piezoelectric resonator, an amplifier, and a variable-capacitance element, the variable-capacitance element is a MOS type capacitance element, one terminal of that is applied with an alternating current voltage, whose intermediate voltage is a V-volt voltage, and the other terminal of that is applied with a control voltage falling within a range whose intermediate value is the V-volt voltage.
2. A piezoelectric oscillator, wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric resonator and the ground, by inserting a MOS type capacitance element in series with the piezoelectric resonator, one end of the MOS type capacitance element is applied with a bias voltage which is the V-volt voltage at an output end or input end of the inverter amplifier and the other end thereof has supplied thereto a control voltage that varies within a range whose intermediate value is the V-volt voltage.
- 25 3. A piezoelectric oscillator, wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal

of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric resonator and the ground, two MOS capacitance elements are inserted respectively on both sides of the piezoelectric resonator; one end of each of the MOS capacitance elements is applied with an alternating current voltage, whose intermediate voltage is a V-volt voltage; and the other end thereof is applied with a control voltage that varies within a range whose intermediate value is the V-volt voltage.

10

4. A piezoelectric oscillator, wherein, in an inverter oscillator in which a piezoelectric element is connected to an input or output end of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric element and the ground, a MOS capacitance element is inserted between the piezoelectric resonator and an input end of the inverter amplifier or between the piezoelectric resonator and an output end of the inverter amplifier; a control voltage Vcont is applied to the terminal on a connection-to-piezoelectric resonator side of the MOS capacitance element; and, when it is assumed that V represents the voltage that is a direct current bias voltage at the input end or output end of the inverter amplifier and that is applied to one end of the MOS capacitance element, it is arranged that said voltage becomes an intermediate voltage of the control voltage Vcont.

PCT EPOL

5. A piezoelectric oscillator, wherein, in an inverter oscillator in which a piezoelectric element is connected to an input or output end of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of  
5 the piezoelectric element and the ground, a MOS capacitance element is inserted between the piezoelectric resonator and an input end of the inverter amplifier or between the piezoelectric resonator and an output end of the inverter amplifier; a control voltage Vcont is applied to the terminal  
10 on the connection-to-piezoelectric resonator side of the MOS capacitance element; and a direct current circuit of a resistor and a capacitor is inserted and connected between the terminal on the inverter-amplifier side of the MOS capacitance element and the input or output terminal of the inverter amplifier;  
15 and further a direct current bias voltage is applied to the terminal on the inverter-amplifier side of the MOS capacitance element.

6. A piezoelectric oscillator according to claim 6, wherein  
20 the amplitude level of an alternating current supplied to the MOS capacitance element is adjusted according to the value of the resistance of the direct current circuit; and when it is assumed that V represents the direct current bias voltage supplied to the terminal on the inverter-amplifier side of the  
25 MOS capacitance element, it is arranged that the direct current bias voltage V becomes an intermediate voltage of the control voltage Vcont.

ABSTRACT OF THE DISCLOSURE

A piezoelectric oscillator is disclosed which falls under the category of an oscillator including a piezoelectric resonator, an amplifier, and a variable-capacitance element.

The variable-capacitance element is a MOS type capacitance element, one terminal of that is fixed at a V-volt voltage, and the other terminal of that is applied with a control voltage falling within a range whose intermediate value is the V-volt voltage. As a result of this, a piezoelectric oscillator is realized which can vary its frequency over a wide range even without use of a minus power supply.

FIG. 1

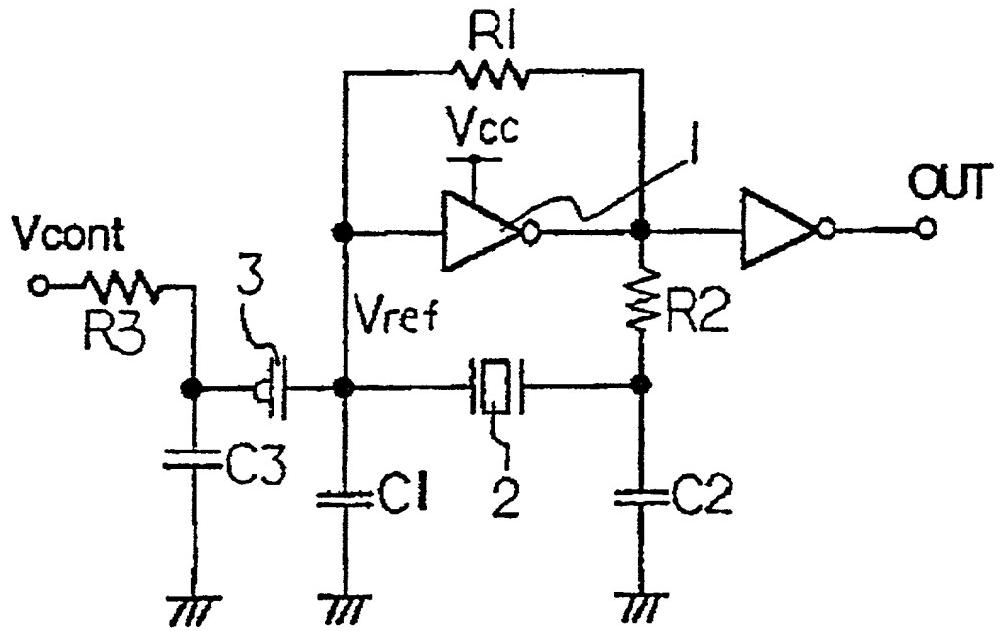


FIG. 2 (a)

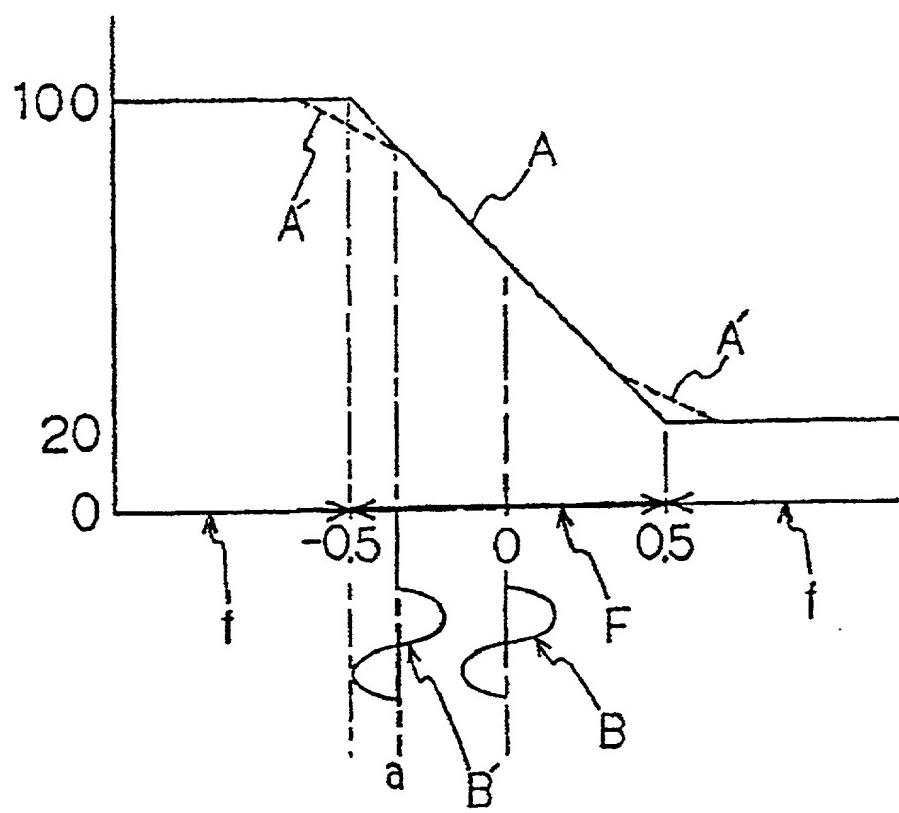


FIG. 2 (b)

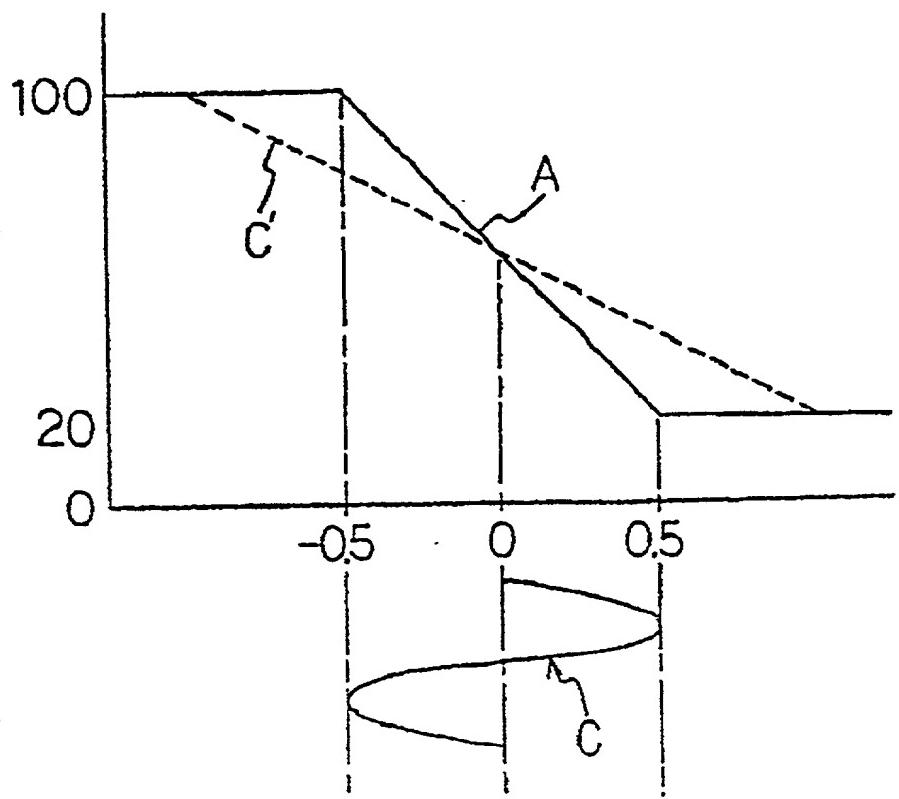


FIG. 3 (a)

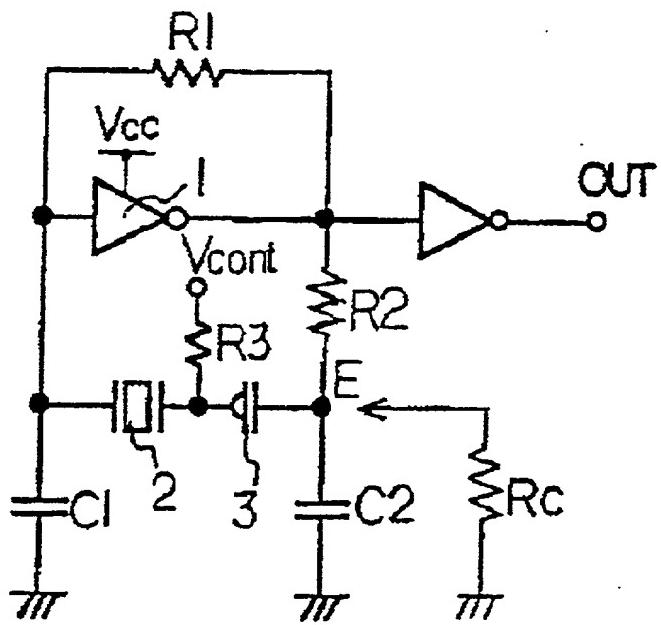


FIG. 3 (b)

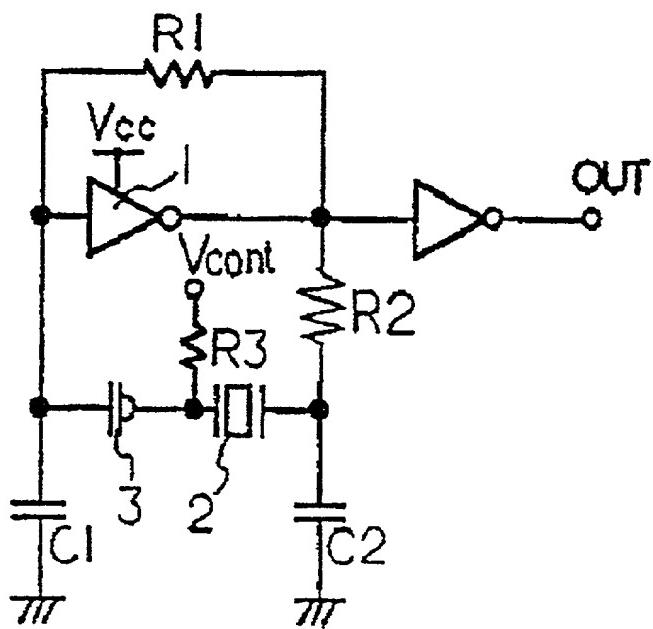


FIG. 4

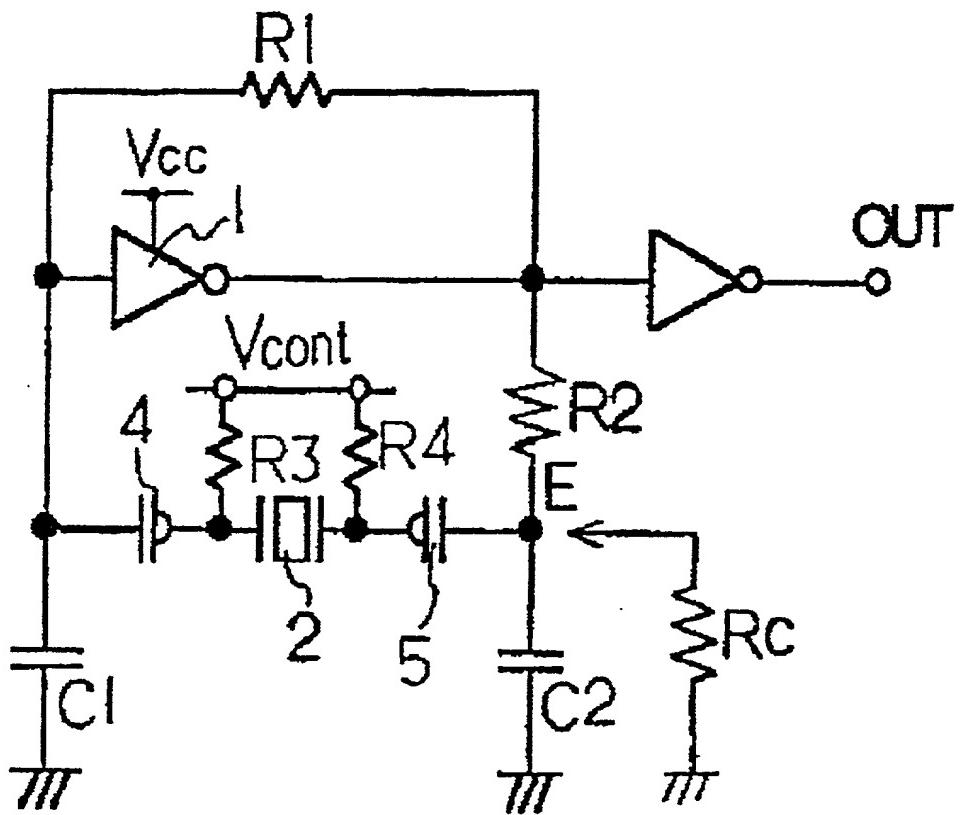


FIG. 5 (a)

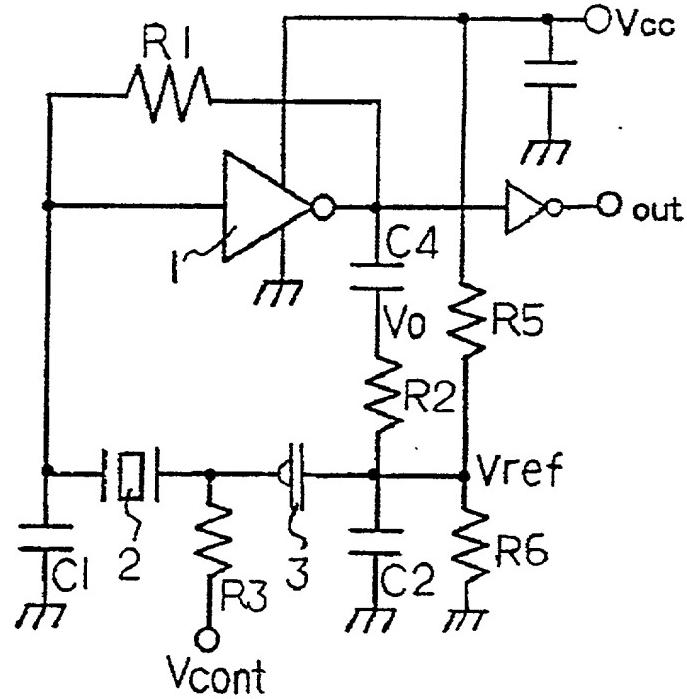


FIG. 5 (b)

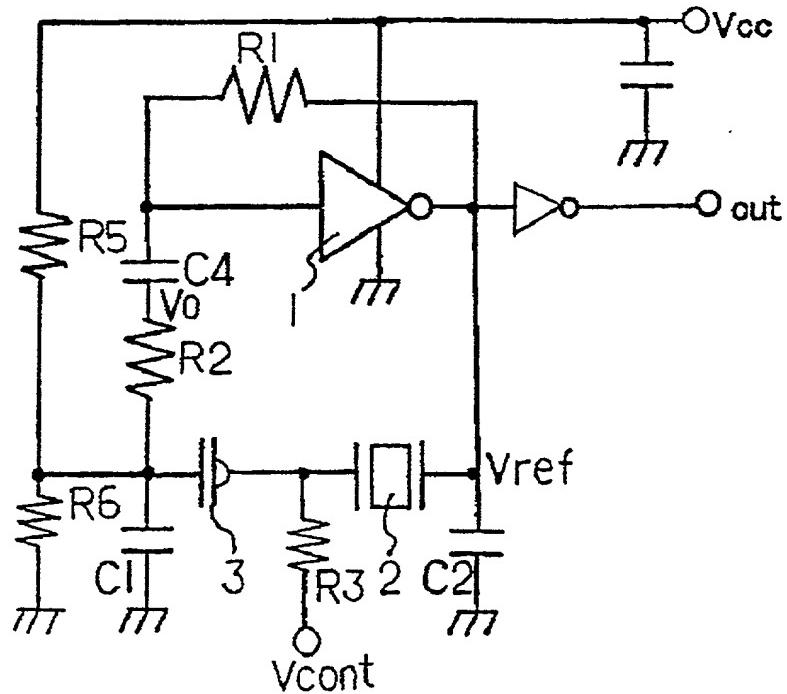


FIG. 6

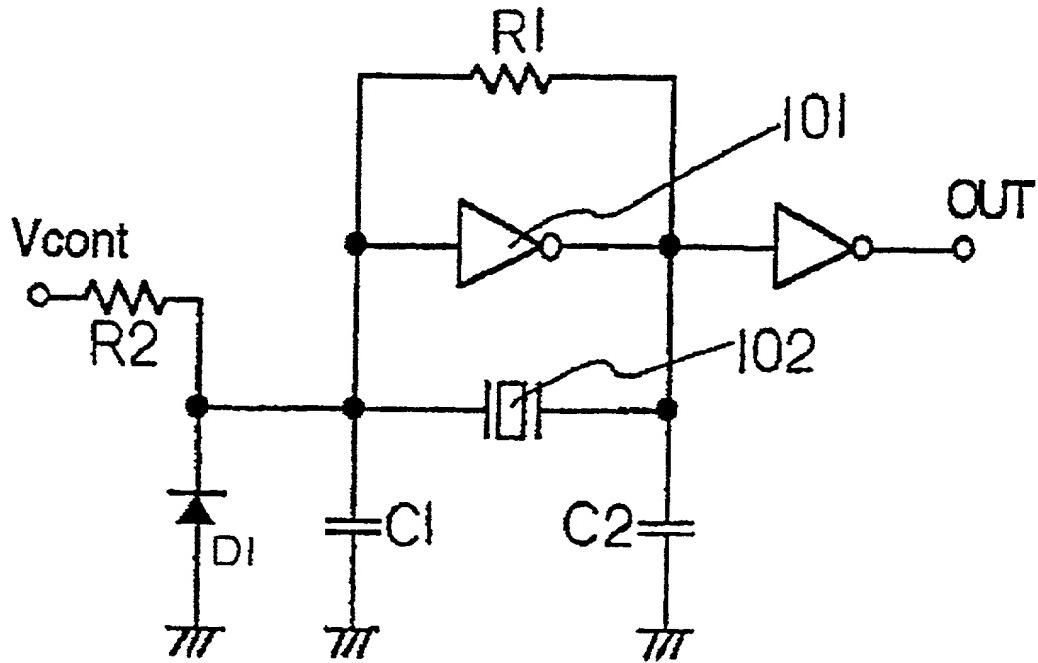


FIG. 7

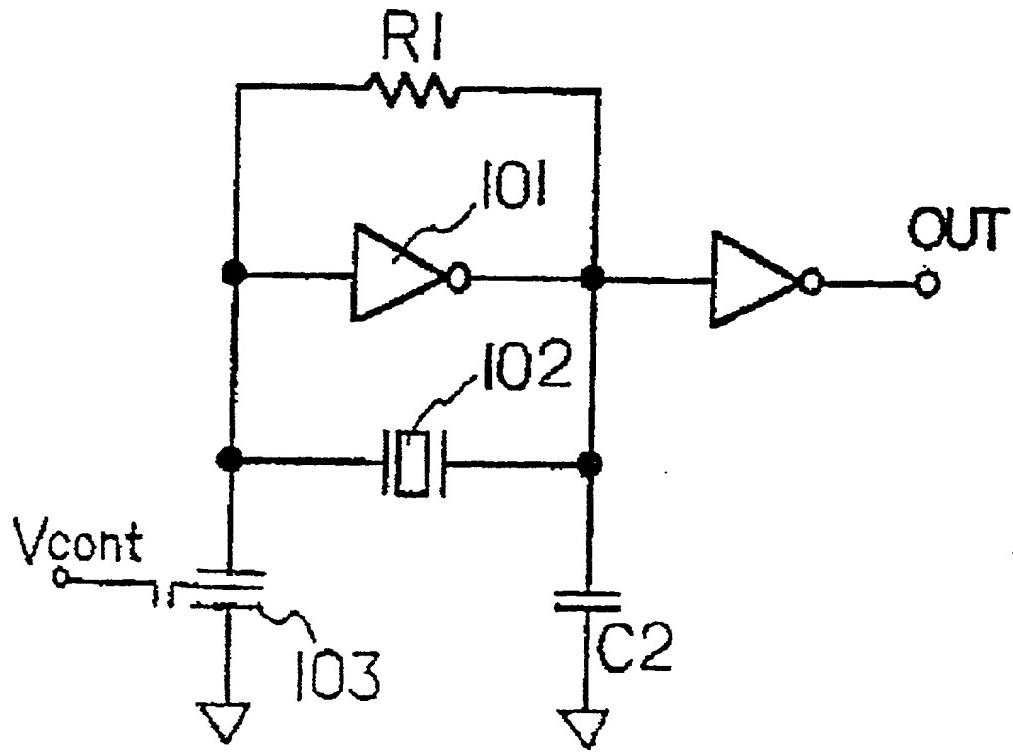


FIG. 8

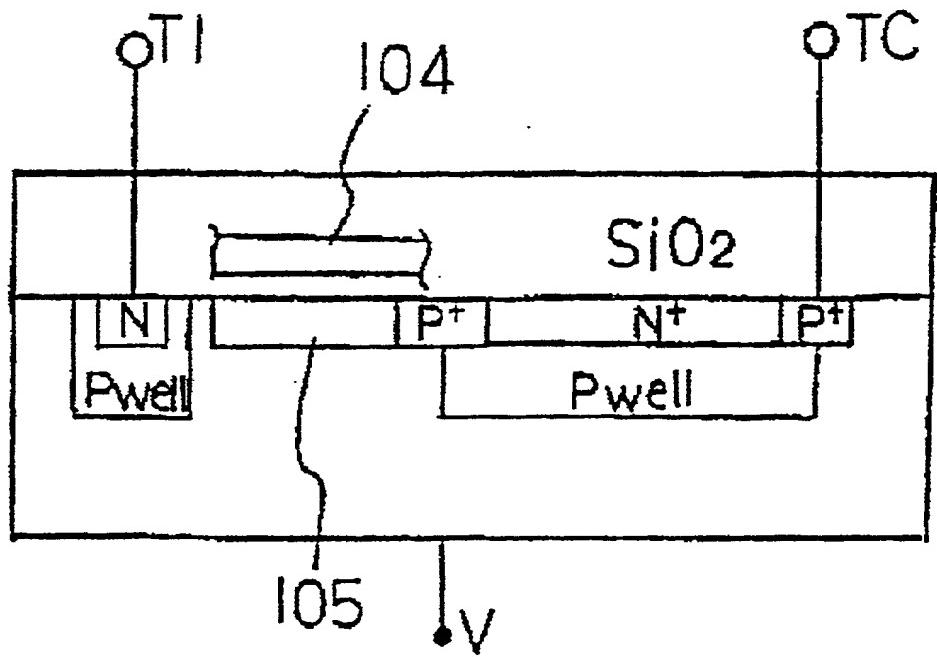
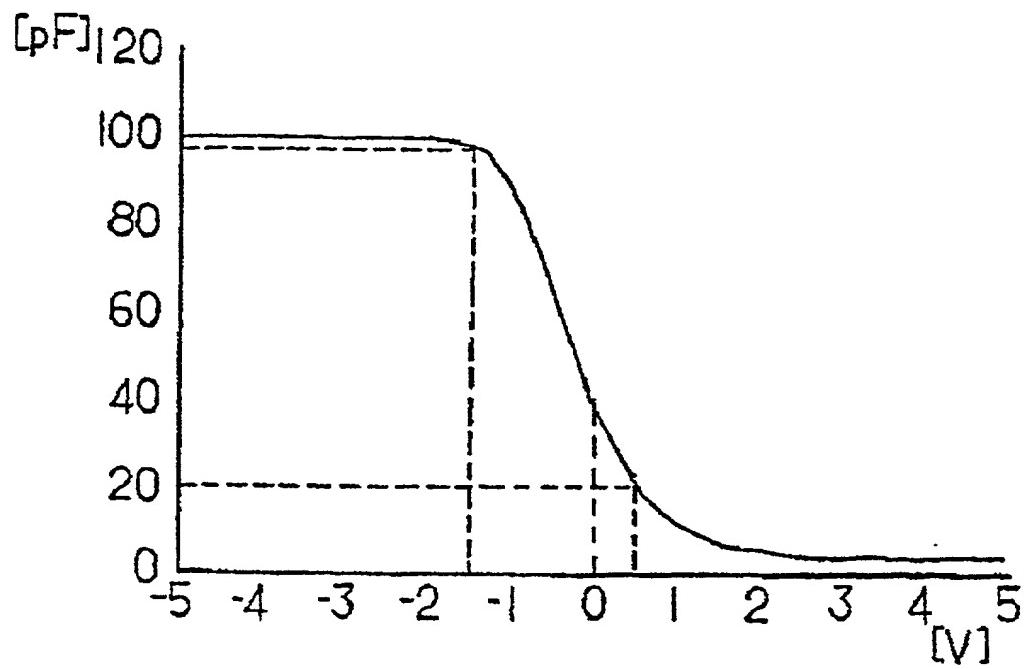


FIG. 9



# DECLARATION AND POWER OF ATTORNEY

PATENT (U.S.A.)  
KCDA & ANDROLIA  
ATTORNEY'S DOCKET NO.  
172A 3003

As a below named inventor, I declare that:

My residence, post office address and citizenship are stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PIEZOELECTRIC OSCILLATOR

the specification of which is attached hereto unless the following box is checked:

was filed on \_\_\_\_\_ as United States Application Number or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or Inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the appropriate line, any foreign application for patent or Inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)					
COUNTRY	APPLICATION NUMBER	Month	DATE OF FILING Day	Year	PRIORITY CLAIMED
Japan	11-289298	10	12	1999	YES <input checked="" type="checkbox"/> NO _____ YES _____ NO _____ YES _____ NO _____ YES _____ NO _____

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

APPLICATION NUMBER	FILING DATE	STATUS - PATENTED, PENDING, ABANDONED

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected herewith.

WILLIAM L. ANDROLIA, REG. NO. 27,177; H. HENRY KODA, Reg. No. 27,729; ALEX CHARTOVE, Reg. No. 31,942.

SEND ALL CORRESPONDENCE TO:			DIRECT TELEPHONE CALLS TO:	
KODA & ANDROLIA 10100 SANTA MONICA BLVD., SUITE 2340 LOS ANGELES, CALIFORNIA 90067			KODA & ANDROLIA (310) 277-1391	

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204	Name of Inventor	FIRST NAME 	LAST NAME 	MIDDLE NAME	Residence CITY 	STATE or COUNTRY 
	Post Office Address					CITIZENSHIP

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements and the like may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE OF INVENTOR 201  Masayuki Ishikawa DATE September 25, 2000	SIGNATURE OF INVENTOR 202  <i>H. Koda</i> DATE September 25, 2000
SIGNATURE OF INVENTOR 203  <i>J. matsu</i> DATE September 25, 2000	SIGNATURE OF INVENTOR 204 

Additional inventors are named on separate Declarations attached hereto.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MASAYUKI ISHIKAWA et al.

For: PIEZOELECTRIC OSCILLATOR

CHANGE OF CORRESPONDENCE ADDRESS

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

Effective September 23, 2000, our office is located at the following address:

**KODA AND ANDROLIA  
2029 Century Park East, Suite 3850  
Los Angeles, CA 90067-3024**

Our telephone and fax numbers remain (310) 277-1391 and (310) 277-4118, respectively. It is therefore respectfully requested that the Patent Office change its records accordingly in connection with the above-identified application.

Respectfully submitted,

KODA AND ANDROLIA

By: 

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